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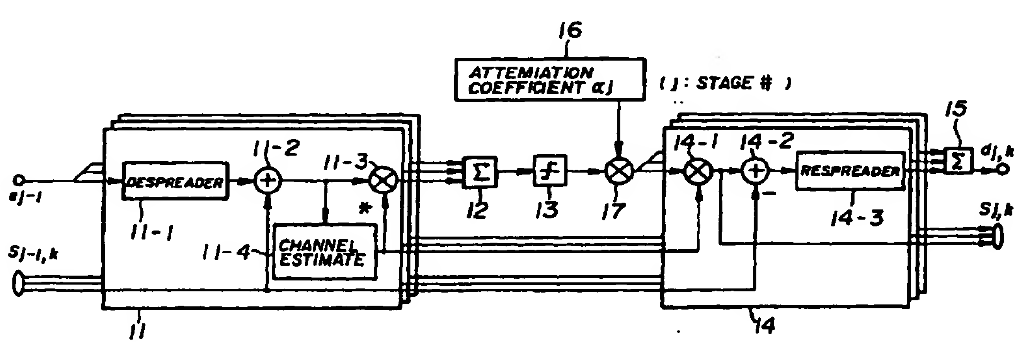
(54) **CDMA Interference canceller**

(57) An interference canceller includes despread processing parts, a combiner combining interference replica generation signals, a decision part that decides an output signal, spread processing parts coupled to the despread processing parts and the decision part, an attenuation coefficient generator generating an attenuation coefficient dependent on a reliability of the interference replica generation signals, and a multiplier multiplying the output signal of the decision part by the attenuation coefficient.

FIG.5



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eration signals are converted into interference replica signals and interference residual signals, which are then transferred to the next stage.

[0015] The provisionally decided symbol Zs^ output by the decision part 93 branches into signals corresponding to the paths. In each of the spread processing parts 94, the multiplier 94-1 multiplies the provisionally decided symbol Zs^ by the channel estimation value ξi^. Hence, the provisionally decided data symbol is decomposed into the signals corresponding to the respective paths, which are output to the next stage as interference replica signals Sj,1 - Sj,k.

[0016] The adders 94-2 of the spread processing parts 94 respectively add the interference replica signals Sj,i - Sj,k that are output by the multipliers 94-1 and correspond to the paths and the interference replica signals Sj-1,1 - Sj-1,k supplied from the previous stage. Then, the adders 94-2 respectively output the differences between the interference replica signals Sj,i - Sj,k of this stage and the interference replica signals Sj-1,i - Sj-1,k. The output signals of the adders 94-2 of the spread processing parts 94 are spread using a spread code in the respective respreaders 94-3. The respread output signals of the respreaders 94-3 corresponding to the respective paths are combined by the combiner 95. The output signals of the combiners 95 of the interference canceller units provided for the respective users' channels are output to the combiner 82 shown in Fig. 1 as interference residual signals dj,1 - dj,k.

[0017] Fig. 3A shows a conventional final-stage receiver provided in the final stage of the multistage type interference canceller, and Fig. 3B shows a frame format. The final-stage receiver labeled 100 in Fig. 3A includes despread processing parts 101, a combiner 102 and a decoder 103.

[0018] The despread processing parts 101 of the final-stage receiver 100 are supplied with the error signal em-1 from the interference replica generation unit of the previous stage and the interference replica signals Sm-1,1 - Sm-1,k, and perform the same process as that of the aforementioned despread processing parts 91 of the interference canceller unit. Hence, received symbols can be obtained.

[0019] Each of the despread processing parts 101 of the final-stage receiver 100 is equipped with a despreader 91-1, an adder 91-2, a multiplier 91-3, and a channel estimation circuit 91-4, which are the same as corresponding those of the despread processing part 91 of the interference canceller unit.

[0020] The combiner 102 of the final-stage receiver 100 performs diversity combining (maximal ratio combining) of the received symbols output from the despread processing parts 101. The resultant receive symbol ΣRiξi^* obtained by the maximal ratio combining is compared with a threshold value by the decoder 103. Hence, a data symbol can be reproduced.

[0021] Referring to Fig. 3B, a pilot symbol 104 is interposed between information symbols 105, and is repeatedly transmitted by a transmitter so that it is located in a given time position. The pilot signal 104 is predetermined known data symbol, and the receive symbol received can be expressed as $Z \cdot \xi$ where Z denotes a value (complex number) of the pilot symbol 104.

[0022] Since the value of the pilot symbol 104 is known, the channel estimate circuit 91-4 multiplies the receive symbol $Z \cdot \xi$ by the complex conjugate Z^* of the value Z of the pilot symbol, and thus outputs $|Z|^2 \cdot \xi$. Since the magnitude (amplitude) of the pilot symbol is known (may be equal to 1: $|Z| = 1$), an estimate value of the transmission path characteristic ξ of the path. The aforementioned channel estimate circuit 91-4 averages the estimated transmission path characteristics ξ obtained using a plurality of pilot symbols. The average value ξ thus obtained is output as the channel estimate value.

[0023] Fig. 4 shows a receiver of a base station including the interference canceller. A signal received via an antenna (ANT) 110 is input to a radio part (Rx) 120, which then amplifies the received signal by means of an amplifier (LNA) 121. The amplified signal is applied to a band-pass filter (BPF) 122, which eliminates components located outside of a given band. A mixer 123 multiplies the output signal of the band-pass filter 122 by a local oscillation signal from a local oscillator LO. Thus, the received signal is converted into a signal in the base band. High-frequency components contained in the base-band signal are eliminated by a low-pass filter (LPF) 124. The output signal of the low-pass filter 124 is then output to the next stage.

[0024] An A/D converter 130 of the next stage samples the received signal from the radio part 120, and outputs a corresponding digital signal, which is applied to a path search circuit 140. The path search circuit 140 calculates delay times of the respective paths by using a plurality of delay waves received, and outputs delay time information obtained for the respective paths to an interference canceller 150.

[0025] The interference canceller 150 performs despreading for the respective paths in the interference replica generation units and the final-stage receivers on the basis of the delay time information obtained for the respective paths. Receive symbols thus obtained are output to decoders 160. Interference between the user channels (spreading codes) and interference between the paths have been eliminated from the receive symbols applied to the decoders.

[0026] Each of the decoders 160 compares the corresponding receive symbol from the interference canceller 150 with a threshold value. Thus, a data symbol can be decoded. Each of the decoders 160 shown in Fig. 4 is the same as the decoder 103 of the final-stage receiver shown in Fig. 3.

[0027] The interference canceller of the above-mentioned type, in which interference is eliminated by subtracting the interference replica signals of the users' channels from the original multiplexed receive signal,

according to a fifth embodiment of the present invention

Fig. 10 is a diagram of an interference canceller unit according to a sixth embodiment of the present invention and

Fig. 11 is a diagram of an interference canceller unit according to a seventh embodiment of the present invention

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0043] Fig. 5 shows an interference canceller unit according to a first embodiment of the present invention. The interference canceller unit shown in Fig. 5 includes despread processing parts 11, a combiner 12, a decision part 13, spread processing parts 14, a combiner 15, an attenuation coefficient generator 16, and a multiplier 17. Each of the despread processing parts 11 includes a despreader 11-1, an adder 11-2, a multiplier 11-3 and a channel estimation circuit 11-4. Each of the spread processing parts 14 includes a multiplier 14-1, an adder 14-2 and a respreader 14-3. The despread processing parts 11 and the spread processing parts 14 are equal in number to received delayed waves, that is, the number of resolvable paths.

[0044] The despread processing parts 11, the combiner 12, the decision part 13, the spread processing parts 14 and the combiner 15 are the same as those of the conventional interference canceller unit shown in Fig. 2, and a description thereof will be omitted.

[0045] The multistage type interference canceller repeatedly performs the interference eliminating process over a plurality of stages. Hence, the precision of the interference replica signals is gradually improved and the interference eliminating performance is thus improved.

[0046] The interference replica signals in the interference canceller unit obtained at an initial stage having a relatively small number of times that the interference eliminating process is repeatedlY carried out have a comparatively low precision. As the number of times that the interference eliminating process is repeatedly carried out is increased, the interference replica signals have an improved precision.

[0047] The attenuation coefficient generator 16 is configured as follows taking into account the above. The attenuation coefficient generator 16 generates different values of the attenuation coefficient for different stages of the interference canceller. The values of the attenuation coefficient used at the initial stages function to greatly attenuate the interference replica signals. As the received signal is transferred over an increased number of stages, the attenuation coefficient has values which apply a reduced attenuation to the interference replica signals. That is, when the attenuation coefficient is denoted as αj (j indicates the stage number), the attenuation coefficient is set so as to have the following values:

$$0 < \alpha 1 < \alpha 2 < \cdots < \alpha j \cdots < \alpha m < 1.$$

[0048] The attenuation coefficient generator 16 generates the attenuation coefficient having the different values for the different stages of the interference canceller and applies it to the multiplier 17. Then, the multiplier 17 multiplies the interference replica signal output by the decision circuit 13 by the attenuation coefficient. Hence, the interference replica signal is attenuated, in each of the spread processing parts 14, by the attenuation coefficient having the value corresponding to the present stage. Hence, it is possible to suppress the influence of the interference replica signals having a comparatively low precision with respect to the interference eliminating process. The attenuation coefficient is multiplied. Hence, as the attenuation coefficient has a smaller value, the degree of attenuation of the interference replica signal is increased.

[0049] Fig. 6 shows an interference canceller unit according to a second embodiment of the present invention. In Fig. 6, parts that are the same as those shown in Fig. 5 are given the same reference numbers and a repetitive description thereof will be omitted.

[0050] The interference canceller unit shown in Fig. 6 includes a path search circuit 21, an attenuation coefficient generator 22, and a multiplier 23. The path search circuit 21 is the same as the path search circuit 140 in the receiver of the base station equipped with the interference canceller. That is, the path search circuit 21 calculates the delay times for the respective paths from the delayed waves received in multiple formation, and outputs delay time information on the respective paths.

[0051] In a general multi-path environment, a path having a large delay has not only a distance attenuation but also reflection and diffraction that take place a plurality of numbers of times. Hence the signal propagated through such a path and then received has a comparatively low received level. Hence, generally, the interference replica having a comparatively large delay of time has a low reliability.

[0052] With the above in mind, the attenuation coefficient generator 22 shown in Fig. 6 generates the attenuation coefficient having values dependent on the delays of time by referring to the delay time information on the paths output by the path search circuit 21. More particularly, the greater the delay time, the smaller the value of the attenuation coefficient αi.

[0053] The multiplier 23 multiplies the interference replica generation signal outputs from the multipliers 14-1 of the spread processing parts 14 corresponding to the respective paths (fingers) by the attenuation coefficient. Hence, the levels of the interference replica signals are attenuated based on the delays of time of the respective paths. Hence, it is possible to suppress the interference replica signals having a low reliability with respect to the interference eliminating process.

and 57-2. Hence, tile levels of the interference replica generation signals are attenuated based on the signal levels or the SIRS respectively obtained for the antenna branches 1 and 2. Hence, it is possible to suppress the influence of the interference replica signal having a low reliability with respect to the interference eliminating process.

[0068] Fig. 10 shows an interference canceller unit according to a sixth embodiment of the present invention. In Fig. 10, parts that are the same as those of the interference canceller unit according to the first embodiment of the present invention are given the same reference numbers, and a repetitive description thereof will be omitted.

[0069] The unit shown in Fig. 6 includes a measurement circuit 61 which measures a signal level or an SIR, an attenuation coefficient generator 62, and a multiplier 63. The measurement circuit 61 measures the signal levels or the SIRs obtained after the demodulation processes carried out by the despread processing parts 11 provided to the respective paths (fingers). The measured values obtained for the respective paths are applied to the attenuation coefficient generator 62. Then, the attenuation coefficient generator 62 generates the attenuation coefficients αi based on the signal levels or the SIRs respectively obtained for the paths (fingers). As the signal levels or the SIRs are lower, the values of the coefficients $\alpha 1$ are smaller.

[0070] The multipliers 63 of the spread processing units 14 multiply the interference replica generation signals from the multipliers 14-1 thereof by the attenuation coefficients αi having the values based on the signal levels or the SIRs obtained for the respective paths (fingers). Hence, the levels of the interference replica generation signals are attenuated based on the signal levels or the SIRS respectively obtained for the paths (fingers). Hence, it is possible to suppress the influence of the interference replica signal having a low reliability with respect to the interference eliminating process.

[0071] Fig. 11 shows an interference canceller unit according to a seventh embodiment of the present invention. In Fig. 11, parts that are the same as those of the interference canceller unit according to the first embodiment of the present invention are given the same reference numbers. and a repetitive description thereof will be omitted.

[0072] The unit shown in Fig. 11 includes a first attenuation coefficient generator 71 and multipliers 72, and includes a second attenuation coefficient generator 74, a multiplier 75 and a measurement circuit 73 which measures signal levels or SIRs after the demodulation, provided in the respective spread processing parts 14.

[0073] The interference canceller unit according to the seventh embodiment corresponds to a combination of the first-embodiment unit shown in Fig. 5 and the attenuation means employed in the sixth-embodiment unit shown in Fig. 10.

[0074] The first attenuation coefficient generator 71 generates attenuation coefficients αj for the respective stages. The multiplier 72 multiplies the interference replica generation signal from the decision part 13 by the attenuation coefficient of the present stage generated by the attenuation coefficient generator 71. Hence, it is possible to attenuate the interference replica generation signal having a low reliability.

[0075] The measurement circuit 73 measures the signal levels or the SIRs of the respective paths (fingers) obtained after the demodulation by the despread processing parts 11. The attenuation coefficient generator 74 generates the attenuation coefficients depending on the measured signal levels or SIRs obtained for the respective paths (fingers). The multipliers 75 multiply the interference replica generation signals by the attenuation coefficients depending on the signal levels or the SIRs respectively obtained for the paths. Hence, the level of the interference replica generation signal having a low signal level or SIR can be attenuated for each path (finger).

[0076] Thus it is possible to suppress, in each stage, the influence of the interference replica signal having a low reliability on the basis of the signal levels or the SIRs.

[0077] It is possible to arbitrarily combine the means for attenuating the interference replica signals having a low reliability employed in the first through sixth embodiments of the present invention and to thus improve the reliability of the interference canceller.

[0078] The present invention includes not only the parallel type shown in Fig. 1 in which the multiple users' channels are processed in parallel formation but also other types. For example, the present invention includes a serial type in which the multiple users' channels are processed in serial formation, a single-stage type and a multiple-stage type.

[0079] The present invention also includes a hard-decision (nonlinear) type interference canceller in which a decision on the received symbol is made to obtain an estimate symbol irrespective of the amplitude of the received symbol, and a soft-decision (linear) type interference canceller in which a decision holding the amplitude of the received signal is made.

[0080] As described above, according to the present Invention, the interference replica signals generated by the interference canceller unit are controlled using at least one of the attenuation coefficients dependent on the stage. the delays of time of paths, the number of users' channels, the levels of the received signals, and the SIRs. Hence, the degree of attenuation of the interference replica signals having a relatively low reliability is increased (the value of the attenuation coefficient is decreased). Hence, it is possible to optimally eliminate interference on the basis of the receive states of the users' channels which are code-multiplexed and to thus improve the transmission quality.

[0081] The present invention is not limited to the specifically disclosed embodiments, and variations and

FIG. 1 PRIOR ART

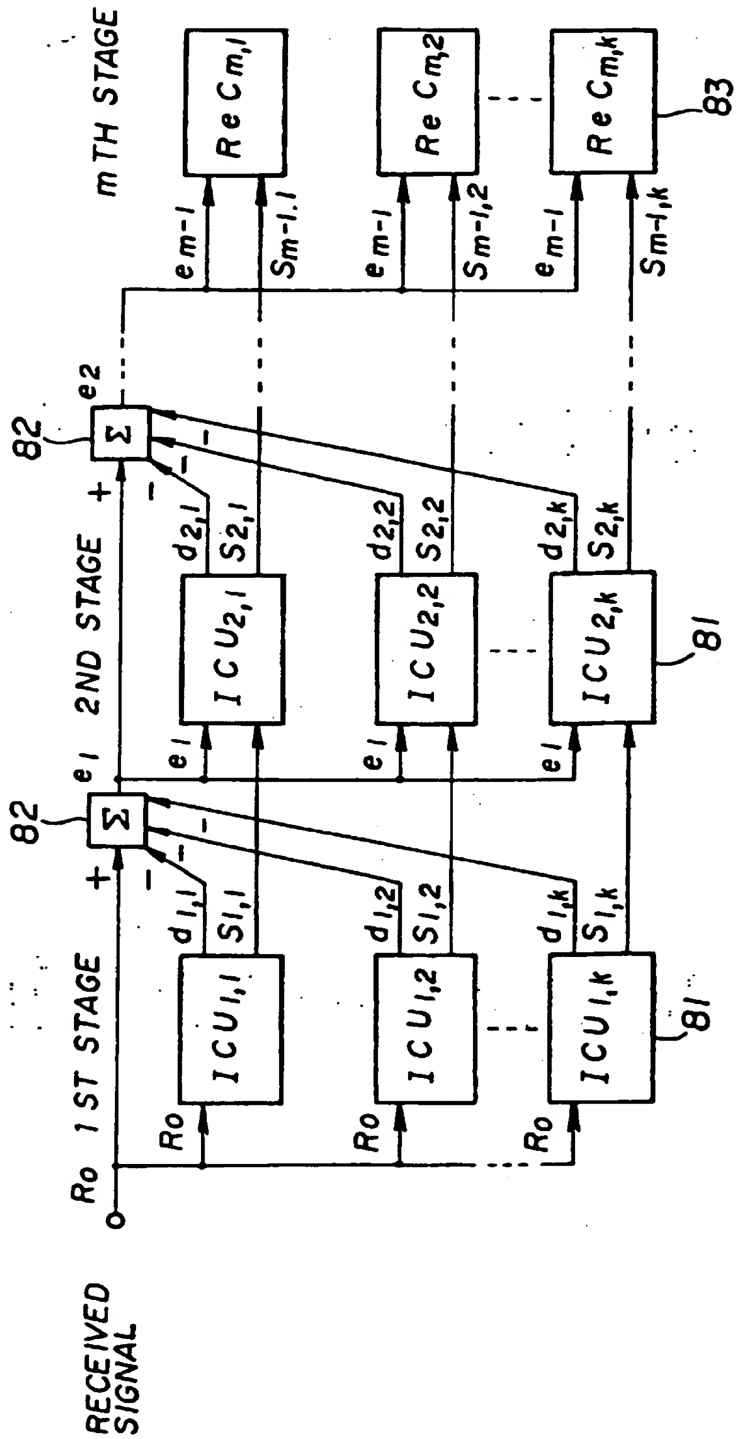

FIG.3A

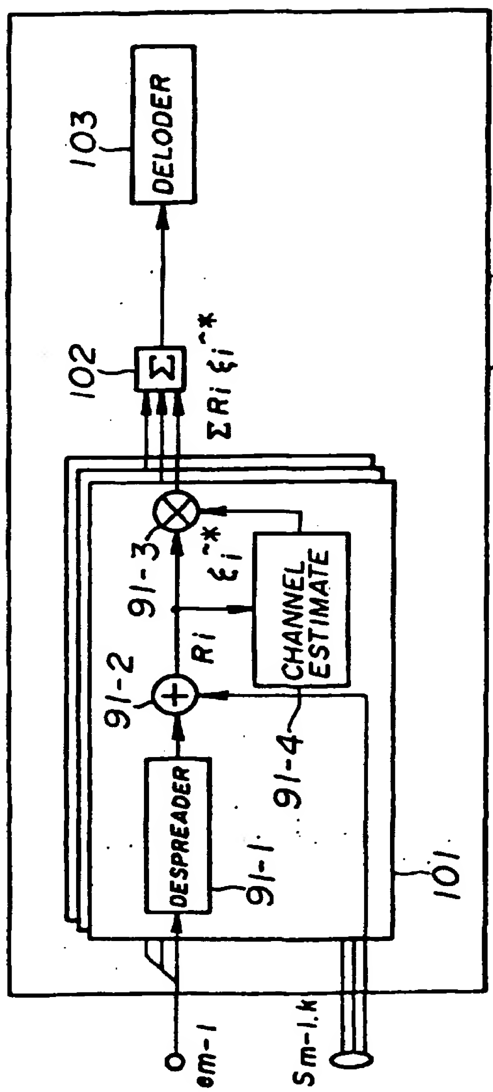
103
DELODER
102
Σ
ΣRi ξi^*
100
91-3
ξi^*
91-2
Ri
CHANNEL ESTIMATE
91-4
DESPREADER
91-1
101
em-1
Sm-1.k

FIG.3B

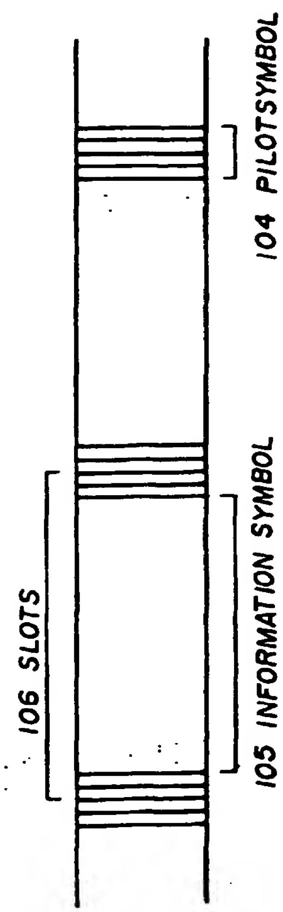
104 PILOTSYMBOL
106 SLOTS
105 INFORMATION SYMBOL

FIG.5

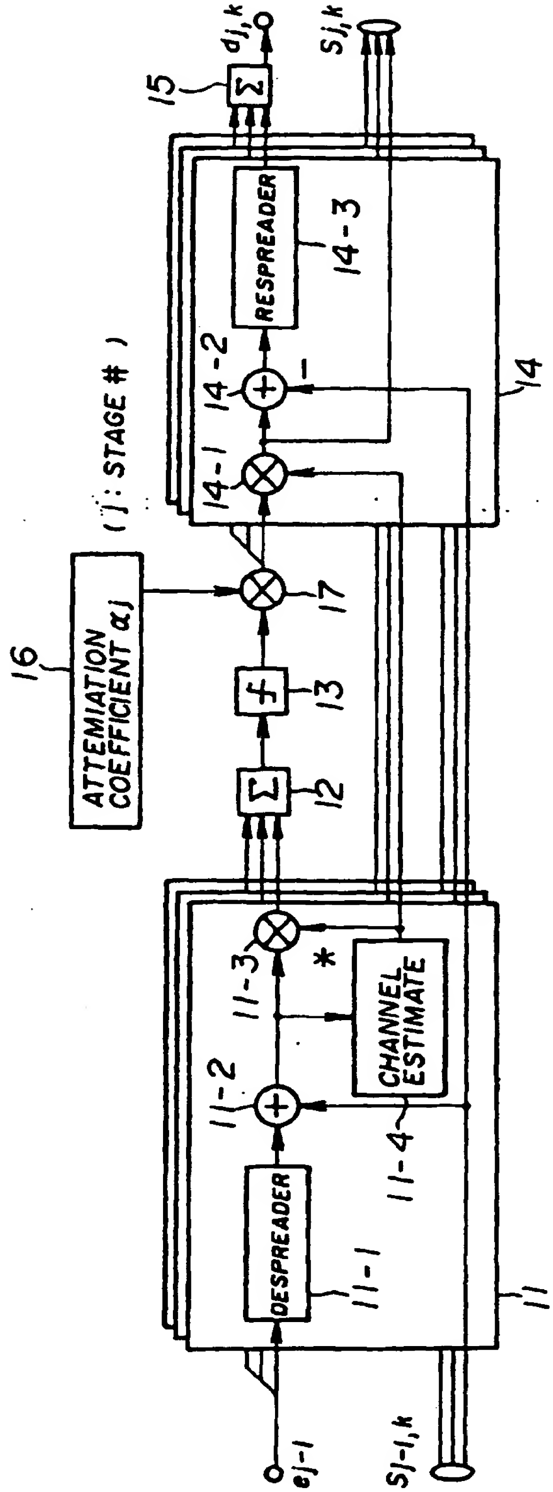
ATTEMIATION COEFFICIENT αj
16
(j : STAGE #)
DESPREADER
CHANNEL ESTIMATE
RESPREADER
11-1
11-2
11-3
11-4
11
12
13
14-1
14-2
14-3
14
15
17
ej-1
Sj-1,k
dj,k
Sj,k
*
-

FIG. 7

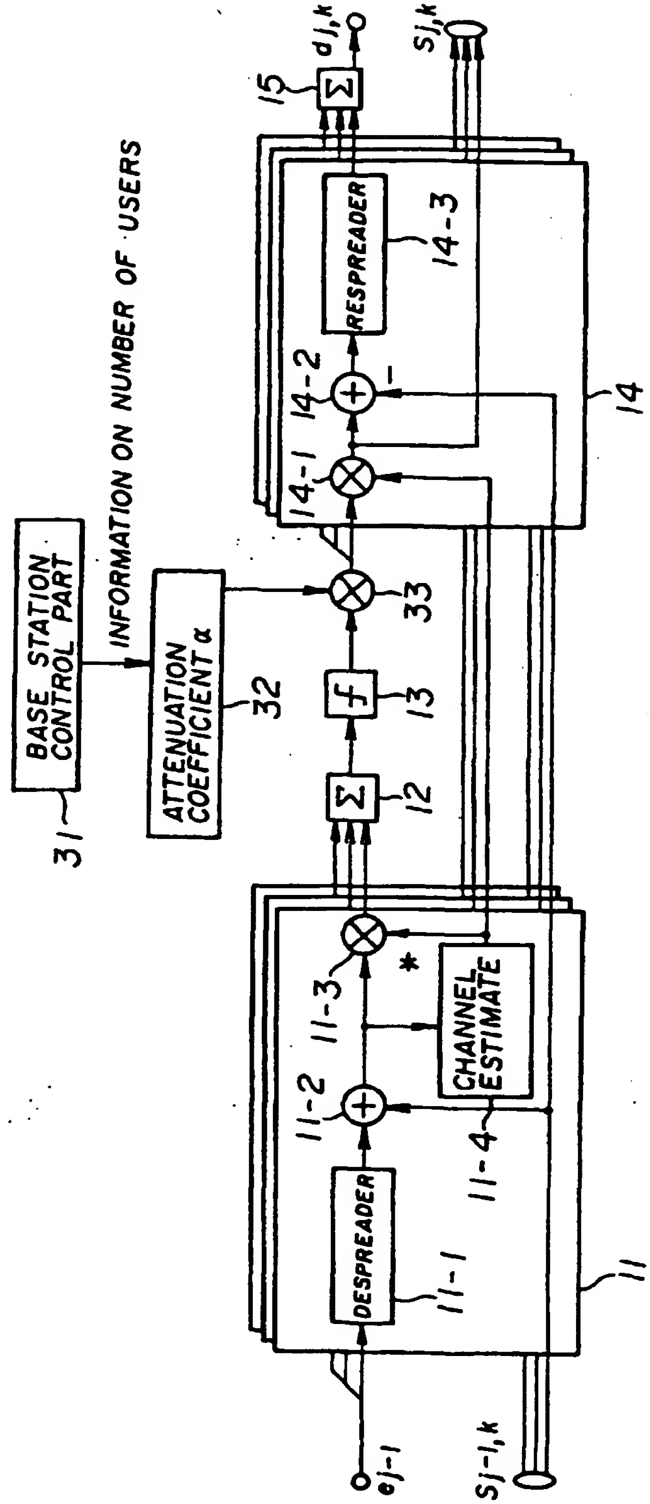
BASE STATION CONTROL PART
31
INFORMATION ON NUMBER OF USERS
ATTENUATION COEFFICIENT α
32
33
DESPREADER
11-1
11-2
11-3
11-4
CHANNEL ESTIMATE
11
Σ
12
∫
13
14-1
14-2
RESPREADER
14-3
14
15
Σ
$d_{j,k}$
$S_{j,k}$
e_{j-1}
$S_{j-1,k}$

FIG. 9

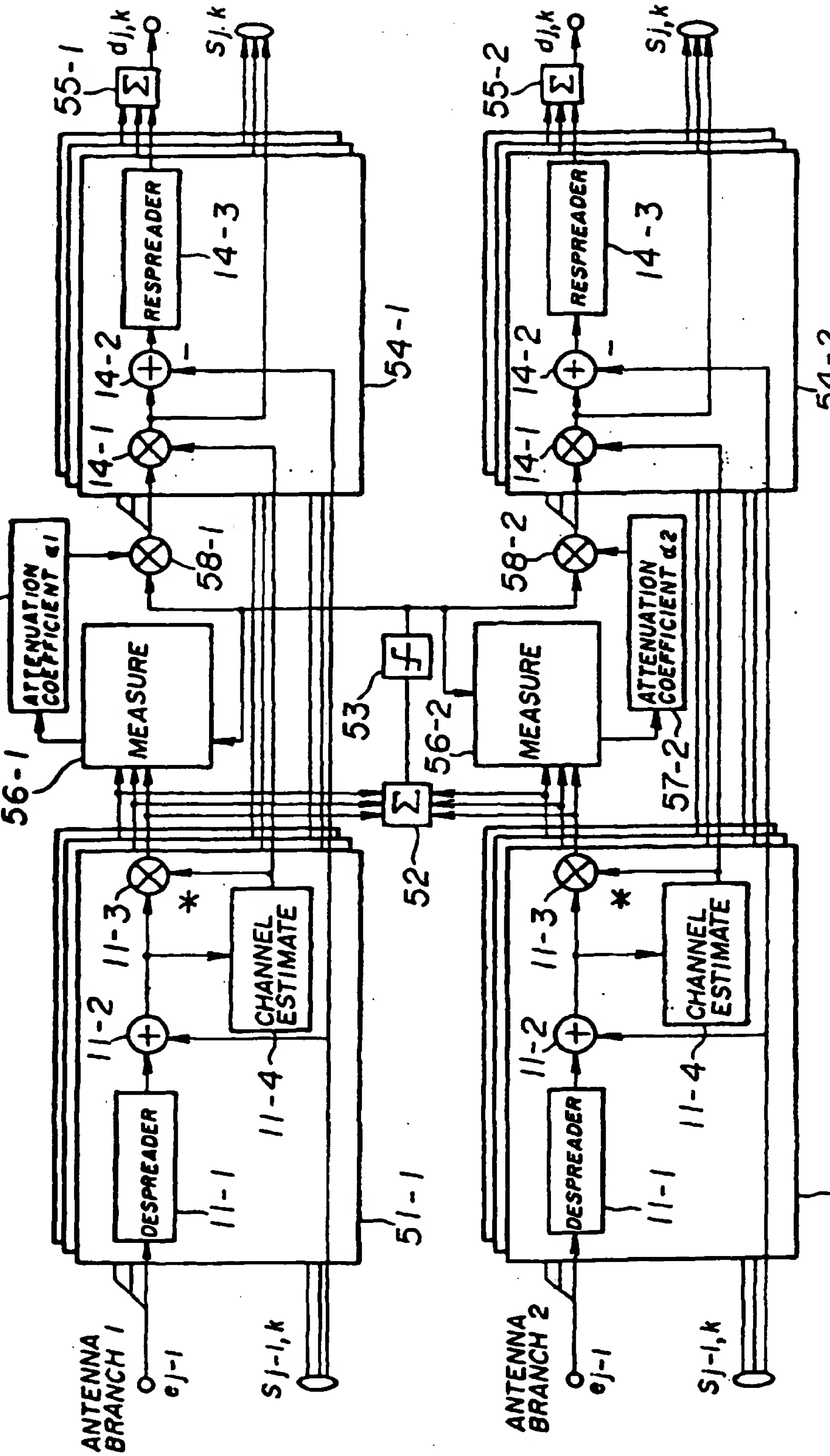
ANTENNA BRANCH 1
ANTENNA BRANCH 2
DESPREADER
CHANNEL ESTIMATE
MEASURE
ATTENUATION COEFFICIENT α1
ATTENUATION COEFFICIENT α2
RESPREADER
11-1
11-2
11-3
11-4
14-1
14-2
14-3
51-1
51-2
52
53
54-1
54-2
55-1
55-2
56-1
56-2
57-1
57-2
58-1
58-2

FIG.11

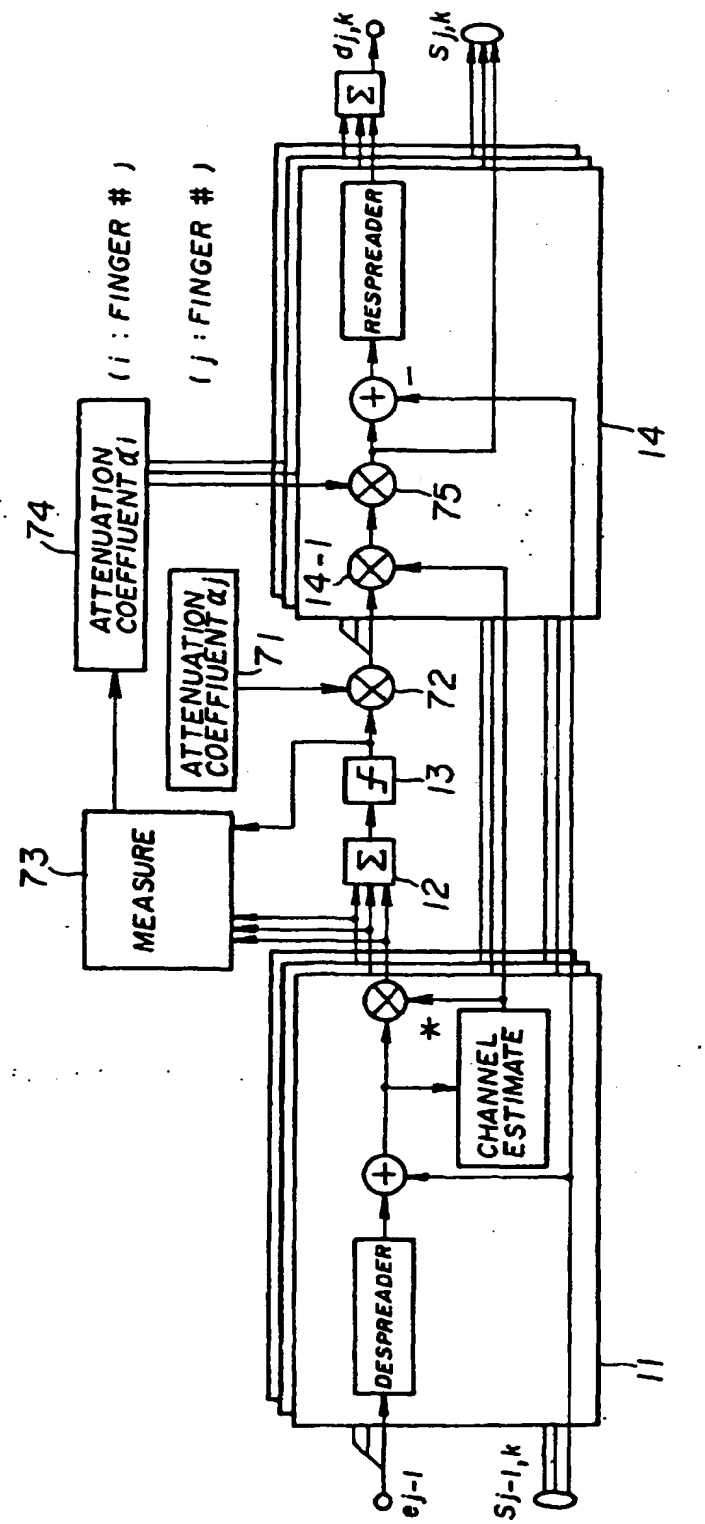
ATTENUATION COEFFIUENT αi
74
(i : FINGER #)
(j : FINGER #)
ATTENUATION COEFFIUENT αj
71
MEASURE
73
DESPREADER
CHANNEL ESTIMATE
*
12
13
72
14-1
75
RESPREADER
14
11
ej-l
Sj-l,k
dj,k
Sj,k

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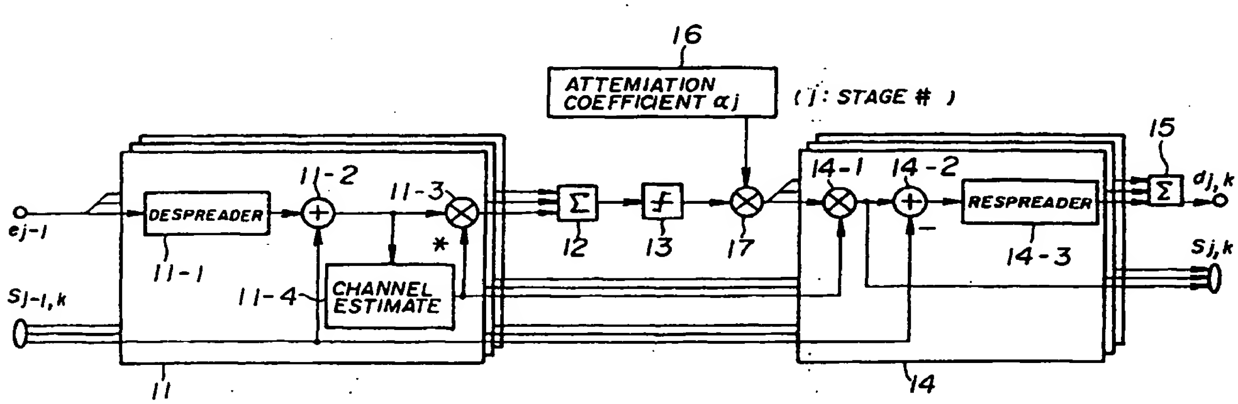
FIG.5



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The members are as contained in the European Patent Office EDP file on
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29-04-2002

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			WO	9642146	A1	27-12-1996
			JP	2855173	B2	10-02-1999
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			AU	695984	B2	27-08-1998
			AU	3654995	A	02-05-1996
			CN	1159870	A	17-09-1997
			EP	0784888	A2	23-07-1997
			WO	9611534	A2	18-04-1996
			JP	11511915	T	12-10-1999
			NO	971543	A	05-06-1997
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			EP	0823796	A2	11-02-1998
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			US	6081516	A	27-06-2000

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